WHAT IS CLAIMED IS:

1. A configuration method of interconnects of a chip, the chip having a power bus, a first metal layer and a plurality of electronic circuits, wherein the first metal layer has a plurality of power lines, and the power lines are substantially parallel and electrically connected to the power bus in parallel, the configuration method comprising:

configuring a plurality of metal lines of a second metal layer of the chip with an automatic place and route process according to the electronic circuits, and at least one sparse area formed on the second metal layer by the automatic place and route process; and

configuring at least one supply-power area in the sparse area and electrically connecting the supply-power area to the power bus, wherein the supply-power area has a plurality of slot areas, and each slot area contains at least one of the metal lines.

2. The configuration method of claim 1, wherein the supply-power area is electrically connected to one of the power lines with at least one via plug, whereby the supply-power is electrically connected to the power bus indirectly.

3. The configuration method of claim 1, wherein the supply-power area is electrically connected to the power bus directly.

4. The configuration method of claim 1, wherein the supply-power area is directly merged with the power bus.

5. The configuration method of claim 1, wherein at least one spacing is between the supply-power area and the metal lines.

6. The configuration method of claim 5, wherein the spacing is not less than a minimum dimension, and the minimum dimension complies with a design rule for unrelated metal-to-metal spacing.

7. The configuration method of claim 1, wherein the supply-power area is a solid metal area.

8. The configuration method of claim 1, wherein the supply-power area is a non-solid metal area.

9. The configuration method of claim 1, wherein the supply-power area is a mesh-like metal area.

10. The configuration method of claim 2, wherein when a quantity of the via plugs vertical to the first metal layer is plural, and the via plugs are directly stacked to connect electrically the supply-power area and one of the power lines.

11. The configuration method of claim 2, wherein when a quantity of the via plugs vertical to the first metal layer is plural, the via plugs are indirectly stacked to connect electrically the supply-power area and one of the power lines.

12. The manufacturing method of claim 1, wherein when a quantity of the second metal layers is two, positions of the two supply-power areas on the two second metal layers substantially correspond to each other to form a capacitor.

13. An interconnection structure of a chip, wherein the chip has a power bus and a plurality of electronic circuits, the interconnection structure comprising:

a first metal layer having a plurality of power lines, wherein the power lines are substantially parallel and electrically connected to the power bus in parallel; and

at least one second metal layer having a plurality of metal lines and at least one supply-power area, wherein the metal lines are configured with an automatic place and route process, and at least one sparse area is formed on the second metal layer, the supply-power area is in the sparse area and electrically connected to the power bus, and the supply-power area has a plurality of slot areas, and each slot area contains at least one of the metal lines.

14. The interconnection structure of claim 13, wherein the supply-power area is electrically connected to one of the power lines with at least one via plug, whereby the supply-power is electrically connected to the power bus indirectly.

15. The interconnection structure of claim 13, wherein the supply-power area is electrically connected to the power bus directly.

16. The interconnection structure of claim 13, wherein the supply-power area is directly merged with the power bus.

17. The interconnection structure of claim 13, wherein at least one spacing is located between the supply-power area and the metal lines.

18. The interconnection structure of claim 17, wherein the spacing is not less than a minimum dimension, and the minimum dimension complies with a design rule for unrelated metal-to-metal spacing.

19. The interconnection structure of claim 13, wherein the supply-power area is a solid metal area.

20. The interconnection structure of claim 13, wherein the supply-power area is a non-solid metal area.

21. The interconnection structure of claim 13, wherein the supply-power area is a mesh-like metal area.

22. The interconnection structure of claim 14, wherein when a quantity of the via plugs vertical to the first metal layer is plural, the via plugs are directly stacked to connect electrically the supply-power area and one of the power lines.

23. The interconnection structure of claim 14, wherein when a quantity of the via plugs vertical to the first metal layer is plural, the via plugs are indirectly stacked to electrically connect the supply-power area and one of the power lines.

24. The interconnection structure of claim 13, wherein when a quantity of the second metal layers is two, the positions of the two supply-power areas on the two second metal layers are substantially corresponding to each other thus forming a capacitor.